WHAT IS CLAIMED IS:

1. A magnetic random access memory comprising:

a memory cell array in which magneto-resistive elements are arranged in a matrix;

a write word line arranged on each row of the memory cell array;

a write bit line arranged on each column of the memory cell array;

a first driver and second driver which are connected to one end of the write word lines respectively, the second driver having a higher driving capability than the first driver;

a first sinker which is connected to the other end of the write word lines;

a pair of third drivers one of which is connected to the write bit lines at one end thereof and the other of which is connected to the write bit lines at the other end thereof;

a pair of fourth drivers one of which is connected to the write bit lines at one end thereof and the other of which is connected to the write bit lines at the other end thereof, the pair of fourth drivers having a higher driving capability than the pair of third driver;

a pair of second sinkers one of which is connected to the write bit lines at one end thereof and the other end of which is connected to the write bit lines at the

other end thereof;

a first circuit configured to cause the second driver and first sinker to write information in a plurality of memory cells at a time by a one-axis writing in an axis of hard magnetization; and

a second circuit configured to cause one of the fourth driver and one of second sinker to write information in a plurality of memory cells by the one-axis writing in an axis of easy magnetization and simultaneously supply a larger current than that in a two-axis write in a normal operation.

2. A memory according to claim 1, further comprising

a column address register which automatically generates write and read column addresses in executing a test, and

a row address register which automatically generates write and read row addresses in executing the test.

3. A memory according to claim 1, further comprising

a column address register which automatically generates a plurality of write column addresses in executing a test,

a column decoder which simultaneously selects a plurality of column addresses,

a row address register which automatically

generates a plurality of write row addresses in executing the test, and

a row decoder which simultaneously selects a plurality of row addresses.

4. A memory according to claim 1, further comprising

a comparator which executes comparison with an expected value after the larger current than that in the two-axis write in the normal operation is supplied,

a first fail register which counts and holds the number of inverted bits or the number of bits on each bit line having a resistance value falling outside standards,

a second fail register which counts and holds the number of bit lines when a value of the first fail register reaches a specific value, and

a third circuit configured to set a fail flag and output a signal from the bit when a value of the second fail register reaches a specific value.

5. A memory according to claim 4, further comprising

a comparator which executes comparison with the expected value simultaneously for memory cells connected to a plurality of bit lines after the larger current than that in the two-axis write in the normal operation is supplied,

fail registers equal in number to the number of

bits to be simultaneously measured, each of the fail registers counting and holding the number of inverted bits or the number of bits on each bit line having the resistance value below the standards,

the second fail register which counts and holds the number of bit lines when the value of the fail register reaches a specific value, and

the third circuit configured to set the fail flag and output the signal from the bit when the value of the second fail register reaches a specific value.

6. A memory according to claim 1, wherein the memory cell comprises one transistor and one magneto-resistive element.

7. A memory according to claim 1, wherein the memory cell is a cross-point memory cell comprising only a magneto-resistive element.

8. A memory according to claim 1, wherein the memory cell is a multilayered-bit-line memory cell comprising one transistor and a plurality of magneto-resistive elements.

9. A test method for a magnetic random access memory, comprising:

executing a write in a memory cell having a magneto-resistive element by a one-axis write along an axis of easy magnetization by a write bit line;

supplying a larger current than that in a two-axis write in a normal operation to a write word line by the

one-axis write along an axis of hard magnetization; and

reading out a resistance value of the memory cell.

10. A method according to claim 9, wherein the write by the one-axis write along the axis of easy magnetization by the write bit line is executed simultaneously for a plurality of memory cells.

11. A method according to claim 9, further comprising, after the read of the resistance value of the memory cell, counting the number of bits each having a shift in asteroid characteristic.

12. A method according to claim 11, further comprising, after counting the number of bits each having the shift in asteroid characteristic, determining whether a count value coincides with a specific value.

13. A method according to claim 12, wherein test is ended when the count value coincides with the specific value.